

NASA Technical Paper 1873

Life Test of a Nickel  
Cadmium Battery With a  
Protection/Reconditioning Circuit

John R. Lanier, Jr., and John R. Bush, Jr.

MAY 1981

CASE FILE  
COPY

**NASA**



NASA Technical Paper 1873

# Life Test of a Nickel Cadmium Battery With a Protection/Reconditioning Circuit

John R. Lanier, Jr., and John R. Bush, Jr.  
*George C. Marshall Space Flight Center  
Marshall Space Flight Center, Alabama*

**NASA**  
National Aeronautics  
and Space Administration

**Scientific and Technical  
Information Branch**

1981



## TABLE OF CONTENTS

	Page
INTRODUCTION .....	1
BACKGROUND .....	1
BPRC OPERATION .....	2
BPRC DESCRIPTION .....	2
BPRC CIRCUIT IMPROVEMENTS AND FUTURE EFFORTS .....	3
TEST RESULTS .....	4
Low Battery Capacity .....	4
Erratic End of Discharge Cell Voltage .....	4
Cell Internal Leakage .....	4
Cell Internal Shorts .....	5
Recharge Fraction Anomaly .....	5
CONCLUSIONS AND RECOMMENDATIONS .....	5
REFERENCES .....	7

## LIST OF ILLUSTRATIONS

Figure	Title	Page
1	Batteries capacity/life history . . . . .	8
2	BPRC schematic diagram. . . . .	9
3	Typical BPRC output characteristic . . . . .	10
4	Revised BPRC schematic diagram . . . . .	11
5	Cell end of discharge anomaly. . . . .	12
6	Cell internal leakage anomaly . . . . .	13
7	Recharge fraction anomaly . . . . .	14

## TECHNICAL PAPER

### LIFE TEST OF A NICKEL CADMIUM BATTERY WITH A PROTECTION/RECONDITIONING CIRCUIT

#### INTRODUCTION

This report is intended as an extension of NASA Technical Note TN D-8508, "A Nickel-Cadmium Battery Reconditioning Circuit" [1]. The work reported therein continued as anticipated. The two batteries under test, which had approximately 18,000 orbital cycles then, have now completed 44,213 orbital cycles in over 8 years of simulated low Earth orbit operation and the test has been terminated. A new, more powerful circuit with higher current diodes (Fig. 5 in TN D-8508), located inside the thermal vacuum chamber within 0.5 m of the batteries to provide protection for weak or shorted cells against reverse polarity, was installed in February 1978. Results of testing during this extended time with the new battery protection and reconditioning circuit (BPRC) that provides both cell protection and battery reconditioning are presented herein.

#### BACKGROUND

The test was begun as a life test of Skylab ATM EPS charger, battery, regulator modules (CBRM). This plan was followed for almost 3500 orbits. The Skylab was launched at that time, and vehicle problems [2] were encountered which impacted the EPS and resulted in significant battery capacity degradation. The anomalous operation was simulated in this test with similar results in battery capacity degradation as shown in Figure 1 between 3000 and 4000 orbits. (Battery capacity as defined in this report is the ampere hours available from the battery at nominal load – approximately 200 watts – when discharged to 1.1 V per cell – 26.4 V for these batteries.) The test was then continued through the end of the Skylab mission simulating onboard operation. Results of that portion of the test, and the test configuration are included in Reference 3. At the end of the Skylab mission in February 1974, the test was converted to simulate battery operation for the proposed Large Space Telescope (LST). Approximately one month later the first reconditioning test, as shown in Figure 1, was performed. The test continued simulating the latest proposed LST depths of discharge (DOD) and later Space Telescope (ST) operations. In October of 1977, after five years of operation, the continuing test began simulation of a 25 kW Power Module (PM) operation with a schedule of programmed load, and thus DOD, variations to simulate three different modes of operation (orbiter on line, 25 percent DOD; Free Flyer Experiment on line, 10 percent DOD; and standby housekeeping loads, 2 percent DOD). The test was terminated December 10, 1980, after 8 years and 2 months of battery operation, with three shorted cells in one battery and two severely degraded cells in the other battery. The BPRC performed well throughout the test, successfully protecting several cells against reversal. Most of the test was run at a temperature of  $10 \pm 5^\circ\text{C}$  with short term operation to as low as  $0^\circ\text{C}$  and as high as  $35^\circ\text{C}$ . Figure 1 is a history of the test showing capacity and orbital life with key events.

## BPRC OPERATION

A circuit similar to Figure 2 was installed on the CBRM's in February of 1978. The output transformers and diodes were mounted inside the thermal/vacuum chamber as close as practical to the CBRMs (within 0.5 m) in order to minimize line drop and enhance cell protection (Section 6 of Figure 2 was duplicated for each CBRM). The outputs were connected to the cells in each CBRM via existing data system cables. The transformer inputs were connected to the remainder of the circuit through spare wires in the respective cable (these wires were not twisted or shielded and were approximately 8 m long, but this caused no problems). The remainder of the circuit was located just outside the chamber at the bulkhead connector approximately 8 m from the battery. The output characteristic of a typical output of the circuit is shown in Figure 3.

The circuit used included a relay controlled load resistor for reconditioning not shown in Figure 3 since the CBRM's had no internal provision for reconditioning. The CBRM's were designed to automatically disconnect the battery from the regulator should the battery voltage drop below 26.4 V, so the BPRC reconditioning resistor was added to provide the capability to further discharge the battery as required for reconditioning.

During the time that this BPRC was connected to the CBRMs, several cell anomalies were observed and several reconditioning cycles were performed as shown on Figure 1. The cell anomalies that occurred resulted in excessive cell discharge and a resultant collapse of cell voltage during battery discharge. The BPRC would maintain the cell voltage at approximately 0.5 V thus preventing cell reversal and damage. This could be observed by watching the cell voltage and/or the BPRC input current. The input current would rise proportional to the number of cells that were collapsed, often indicating problems that could not have been detected in a normal system where every cell could not be monitored. The "state of health" of the battery could thus be determined by monitoring the BPRC input current. As the test continued and the cells grew weaker (especially during the last 12 months), three cells in one battery shorted completely and two cells in the other battery continuously collapsed during discharge.

Reconditioning cycles were aperiodically performed as shown on Figure 1. This was done by connecting the reconditioning resistor across the battery terminals, allowing the battery to completely discharge, and letting the BPRC hold each cell at approximately 0.5 V as they collapsed. The battery would be held at 0.5 V per cell for usually 2 to 3 days. Test data showed that this length of time was sufficient for the cells to regain most of their capacity. Longer times (up to 6 days) resulted in very little more capacity recovery. For the batteries tested, reconditioning for less than 24 hr resulted in a short term voltage enhancement only (Reference 1, Figure 7). Therefore, a 40 to 48 hr period with all cells below 0.6 to 0.7 V is recommended for reconditioning. However, each battery should be tested, and with the higher discharge rates allowed by the new BPRC shorter reconditioning times may be possible.

## BPRC DESCRIPTION

Section 1 of Figure 2 is an input filter and a series pass regulator that supplies 12 V to the control logic.



Section 2 is the main control logic. The CD4047AE generates a 40 kHz signal that is shaped to produce a series of short, negative pulses. These pulses are used to trigger the LM555 timer whose output pulses are a function of the input voltage -- as the input voltage rises, the pulses get longer. Each pulse from the LM555 causes both output transistors to turn off. The purpose of this is two fold: it prevents both transistors from ever being on at the same time, thus preventing high current spikes that could damage the transistors; and it provides regulation at the output should the input voltage vary. Also, the LM111 comparator can lengthen these pulses should the input current go too high. This feature provides a current limiting capability to keep from damaging the circuit should it be turned on into a battery with several shorted cells or a completely discharged battery. As the cells on a discharged battery are charged by the BPRC outputs, the high input current (which would initially be necessary to charge these cells) would gradually decrease and the BPRC would resume normal operation. The input pulses to the LM555 are also delayed, inverted, and used to clock a flip-flop that selects which output transistor will turn on next.

Section 3 is an enable circuit that allows operation only when the input voltage is above 15 V. Section 4 also receives this enable signal and pulses an initial voltage to the 1  $\mu$ f capacitors to insure that a good start voltage is present.

Section 5 is the driver stage. A proportional forced beta configuration is used for efficiency. Most of the time the BPRC is operating under no load. With a proportional drive configuration there is no excess base drive to the power transistors, and minimal power loss occurs.

Section 6 is the output circuit which consists of an input filter choke, isolation diodes, and an output transformer with a bifilar wound full wave rectified low voltage output winding for each cell. During operation, the BPRC is isolated from normal cells (since the output diodes are reverse biased) and only those cells which have collapsed or shorted will draw power from the circuit. If all cells are operating normally, the BPRC will use a standby power of only 3 W.

## BPRC CIRCUIT IMPROVEMENTS AND FUTURE EFFORTS

The circuit shown in Figure 4 has recently been completed. The power transistors have been replaced with state-of-the-art high power field-effect transistors which increase efficiency and significantly simplify the drive circuitry. The output transformer cores have been replaced with ferrite cores which provide superior performance when several transformers are driven by common drive transistors as required when more than one battery or battery module is protected by one BPRC. This is due to inherent characteristics (higher magnetizing current and detectable current imbalance before saturation) of ferrite cores. State-of-the-art high power Schottky diodes are also being used in the outputs. (Experience with high power Schottky diodes in this circuit indicates the need for screening to insure that they can withstand a reverse surge of approximately 1 mj at 10 A. This is necessary because of significant parasitic inductances in the BPRC secondaries. Some diode manufacturers are now adding internal protection to their Schottky diodes which may eliminate this requirement in the future.) This circuit is being tested in a high voltage battery in a 25 kW Power Module Breadboard at MSFC.

1. REPORT NO. NASA TP-1873	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.	
4. TITLE AND SUBTITLE Life Test of a Nickel Cadmium Battery With a Protection/Reconditioning Circuit		5. REPORT DATE May 1981	
		6. PERFORMING ORGANIZATION CODE	
7. AUTHOR(S) John R. Lanier, Jr., and John R. Bush, Jr.		8. PERFORMING ORGANIZATION REPORT #	
9. PERFORMING ORGANIZATION NAME AND ADDRESS George C. Marshall Space Flight Center Marshall Space Flight Center, Alabama 35812		10. WORK UNIT NO. M-350	
		11. CONTRACT OR GRANT NO.	
12. SPONSORING AGENCY NAME AND ADDRESS National Aeronautics and Space Administration Washington, D. C. 20546		13. TYPE OF REPORT & PERIOD COVERED  Technical Paper	
		14. SPONSORING AGENCY CODE	
15. SUPPLEMENTARY NOTES Prepared by Electronics and Control Laboratory, Science and Engineering			
16. ABSTRACT  <p>This report discusses the results of a Ni-Cd battery test over a period of 8 years, 2 months and 44,213 simulated low earth orbits. The battery cells were protected against overdischarge and reversal at discharge rates up to 25 amperes (1.25C) by a battery protection and reconditioning circuit (BPRC). The circuit performed flawlessly during the test, and proved its value, both as a battery reconditioner and a cell protection device. Battery cell failures are also discussed. The test demonstrated the viability of using Ni-Cd batteries at depths-of-discharge up to 25 percent for over 5 years in a low Earth orbit.</p>			
17. KEY WORDS  Ni-Cd battery, Electrical Power System (EPS), battery reconditioning, cell protection, low Earth orbit		18. DISTRIBUTION STATEMENT  Unclassified - Unlimited   Subject Category 20	
19. SECURITY CLASSIF. (of this report) Unclassified	20. SECURITY CLASSIF. (of this page) Unclassified	21. NO. OF PAGES 18	22. PRICE A02

Section 2 is the main control logic. The CD4047AE generates a 40 kHz signal that is shaped to produce a series of short, negative pulses. These pulses are used to trigger the LM555 timer whose output pulses are a function of the input voltage — as the input voltage rises, the pulses get longer. Each pulse from the LM555 causes both output transistors to turn off. The purpose of this is two fold: it prevents both transistors from ever being on at the same time, thus preventing high current spikes that could damage the transistors; and it provides regulation at the output should the input voltage vary. Also, the LM111 comparator can lengthen these pulses should the input current go too high. This feature provides a current limiting capability to keep from damaging the circuit should it be turned on into a battery with several shorted cells or a completely discharged battery. As the cells on a discharged battery are charged by the BPRC outputs, the high input current (which would initially be necessary to charge these cells) would gradually decrease and the BPRC would resume normal operation. The input pulses to the LM555 are also delayed, inverted, and used to clock a flip-flop that selects which output transistor will turn on next.

Section 3 is an enable circuit that allows operation only when the input voltage is above 15 V. Section 4 also receives this enable signal and pulses an initial voltage to the 1  $\mu$ f capacitors to insure that a good start voltage is present.

Section 5 is the driver stage. A proportional forced beta configuration is used for efficiency. Most of the time the BPRC is operating under no load. With a proportional drive configuration there is no excess base drive to the power transistors, and minimal power loss occurs.

Section 6 is the output circuit which consists of an input filter choke, isolation diodes, and an output transformer with a bifilar wound full wave rectified low voltage output winding for each cell. During operation, the BPRC is isolated from normal cells (since the output diodes are reverse biased) and only those cells which have collapsed or shorted will draw power from the circuit. If all cells are operating normally, the BPRC will use a standby power of only 3 W.

## **BPRC CIRCUIT IMPROVEMENTS AND FUTURE EFFORTS**

The circuit shown in Figure 4 has recently been completed. The power transistors have been replaced with state-of-the-art high power field-effect transistors which increase efficiency and significantly simplify the drive circuitry. The output transformer cores have been replaced with ferrite cores which provide superior performance when several transformers are driven by common drive transistors as required when more than one battery or battery module is protected by one BPRC. This is due to inherent characteristics (higher magnetizing current and detectable current imbalance before saturation) of ferrite cores. State-of-the-art high power Schottky diodes are also being used in the outputs. (Experience with high power Schottky diodes in this circuit indicates the need for screening to insure that they can withstand a reverse surge of approximately 1 mj at 10 A. This is necessary because of significant parasitic inductances in the BPRC secondaries. Some diode manufacturers are now adding internal protection to their Schottky diodes which may eliminate this requirement in the future.) This circuit is being tested in a high voltage battery in a 25 kW Power Module Breadboard at MSFC.

Future efforts will include further circuit improvement, a packaging study, better methods of connecting the BPRC outputs to the individual cells, and eventual development of a flight qualified unit.

## **TEST RESULTS**

The two test batteries, part No. 40M26202, serial No. 80 and serial No. 84, were designated battery No. 1 and No. 2, respectively, in Reference 1 and in this report. Both batteries successfully supplied loads demanding depths of discharge (DOD) of up to 25 percent for almost eight years. Only after a third cell shorted in battery 1 at 39,040 orbits and over 7 years of operation was the battery unable to supply the full load, and then only because the CBRM regulator would trip off at 26.5 V on the battery. However, several types of anomalies occurred and each is discussed below.

### **Low Battery Capacity**

As discussed in Reference 1 and shown in Figure 1, the batteries suffered an abnormal loss of capacity while simulating ATM flight problems at approximately 3500 orbits. Subsequent reconditioning restored the capacity, and demonstrated the usefulness of a flight reconditioning circuit.

### **Erratic End of Discharge Cell Voltage**

This behavior first occurred on cell 23 of battery 2 as shown in Figure 5 where it is compared to a normal cell. Similar problems occurred later on cell 12 of battery 1 and cell 24 of battery 2. A reconditioning cleared the problem as noted in Reference 1, but similar or other problems occurred at later dates. Ultimately two of these cells, cell 12 in battery 1 and cell 23 in battery 2, failed although they were not the first cell in either battery to fail. The cause of this behavior is not known but a cell analysis currently in progress may provide insight into the problem.

### **Cell Internal Leakage**

Cells 12 and 17 of battery 1 and cells 16, 23 and 24 of battery 2 exhibited evidence of internal cell leakages of 5 A or more. These cells were prevented from discharging below approximately 0.5 V by the battery protection circuit and subsequently recovered. The time to recovery varied from two orbits to 1700 orbits. The degree of leakage varied from a minimum level that would cause the cell voltage to drop near the end of discharge to a maximum level that would cause the cell voltage to drop to 0.5 V as soon as charge was terminated. An example of these two conditions is shown in Figure 6. Leakage that was great enough to prevent the cell from making a significant contribution to the load was considered a cell failure until the cell recovered. This was the final failure mode of cells 16 and 23 in battery 2. At the end of the test both of these cells had less than 0.5 A-hr of effective capacity. Note that these cells did exhibit normal or near normal voltage during charge. The final failure of cell 16 occurred at 41,210 orbits. The final failure of cell 23 occurred at 42,470 orbits. All of these cells except cell 24 were failed at the end of the test. However, these anomalies do show the positive contribution of a cell protection circuit since the cells did recover for appreciable periods of time, and did not fail catastrophically so that the entire battery was lost.

### **Cell Internal Shorts**

Cells 12, 17, and 21 in battery 1 failed with internal shorts. The difference in this failure mode and the previous internal leakage failure mode may be only in degree. The shorted cells had no voltage output during charge or discharge, and thus resulted in somewhat higher cell charge voltage on the good cells. This could have caused greater stress on these cells and may have contributed to a more rapid degradation of this battery. The fore-mentioned cell analysis may reveal the difference in these two failure modes. Cell 21 failed at 32,340 orbits, cell 12 failed at 33,280 orbits, and cell 17 failed at 39,040 orbits.

### **Recharge Fraction Anomaly**

Battery 1 exhibited a recharge fraction anomaly that was discussed briefly in Reference 1. The anomaly resulted in the recharge fraction of the battery gradually increasing from 108 percent to 118 percent over a period of time. Reconditioning the battery resulted in a lowering of the recharge fraction and a repeat of the cycle as shown in Figure 7. This anomaly caused the battery to operate at a temperature approximately 4 °C higher than battery 2, and may account for the somewhat more severe degradation in battery 1. This anomaly is particularly perplexing since the recharge fraction of these batteries was controlled by cell third electrodes (oxygen recombination electrode). There are three cells in each battery with active third electrodes, any one of which could terminate charge. All three third electrodes in each battery seemed to function properly and remain matched throughout the test. However, all three electrodes in battery 1 demonstrated the delayed output that resulted in high recharge fraction while none of the battery 2 electrodes ever demonstrated this characteristic. The cell analysis program may reveal the cause of this difference.

## **CONCLUSIONS AND RECOMMENDATIONS**

This test empirically demonstrated several key principles relative to operation of large electrical power systems in low earth orbit. These principles may also be generally applicable to geosynchronous earth orbit as well as other types of operation in space. The principles are:

- 1) With proper design and charge control techniques a Ni-Cd battery can be expected to operate for significantly more than 5 years in low earth orbit. This is true even at significant depths of discharge. Most of this test was performed at 25 percent DOD.
- 2) Provision to recondition a Ni-Cd battery is simple to incorporate in the electrical power system, and provides a powerful tool for use against known degradation modes as well as surprise losses of capacity.
- 3) Provision to protect Ni-Cd battery cells against a variety of cell anomalies that could lead to cell reversal and subsequent battery loss is also relatively simple. It does require a higher power circuit and layout consideration to minimize wire lengths. However, a circuit that accomplishes this will also provide reconditioning, and thus is a BPRC as described herein.

Based on these results and conclusions, the following recommendations are presented:

- 1) Consider Ni-Cd batteries as viable candidates for energy storage elements for up to 5 years in low earth orbit at temperatures of 0 to 15°C and depths of discharge of up to 25 percent.

- 2) Provide a BPRC for battery reconditioning and cell protection for any mission over six months. This becomes increasingly important as the length of time increases and as the numbers of cells in series increases. The circuit presented herein has been shown effective for Ni-Cd batteries of up to 112 series cells and 60 A-hr capacity. With the capability provided by the BPRC to protect against 10 percent or more cell failures and provide an indication of the number of shorted cells for charge control modification, a Ni-Cd battery life in low Earth orbit approaching 10 years may be reasonable.

## REFERENCES

1. Lanier, J. Roy, Jr.: A Nickel-Cadmium Battery Reconditioning Circuit. NASA TN D-8508, June 1977.
2. Woosley, A. P.: MSFC Skylab Electrical Power Systems Mission Evaluation. NASA TM X-64818, June 1974, Skylab Program Office.
3. Lanier, J. Roy, Jr.: CBRM Life Test II Report. MSFC 40M22431, November 1974, Power Branch.

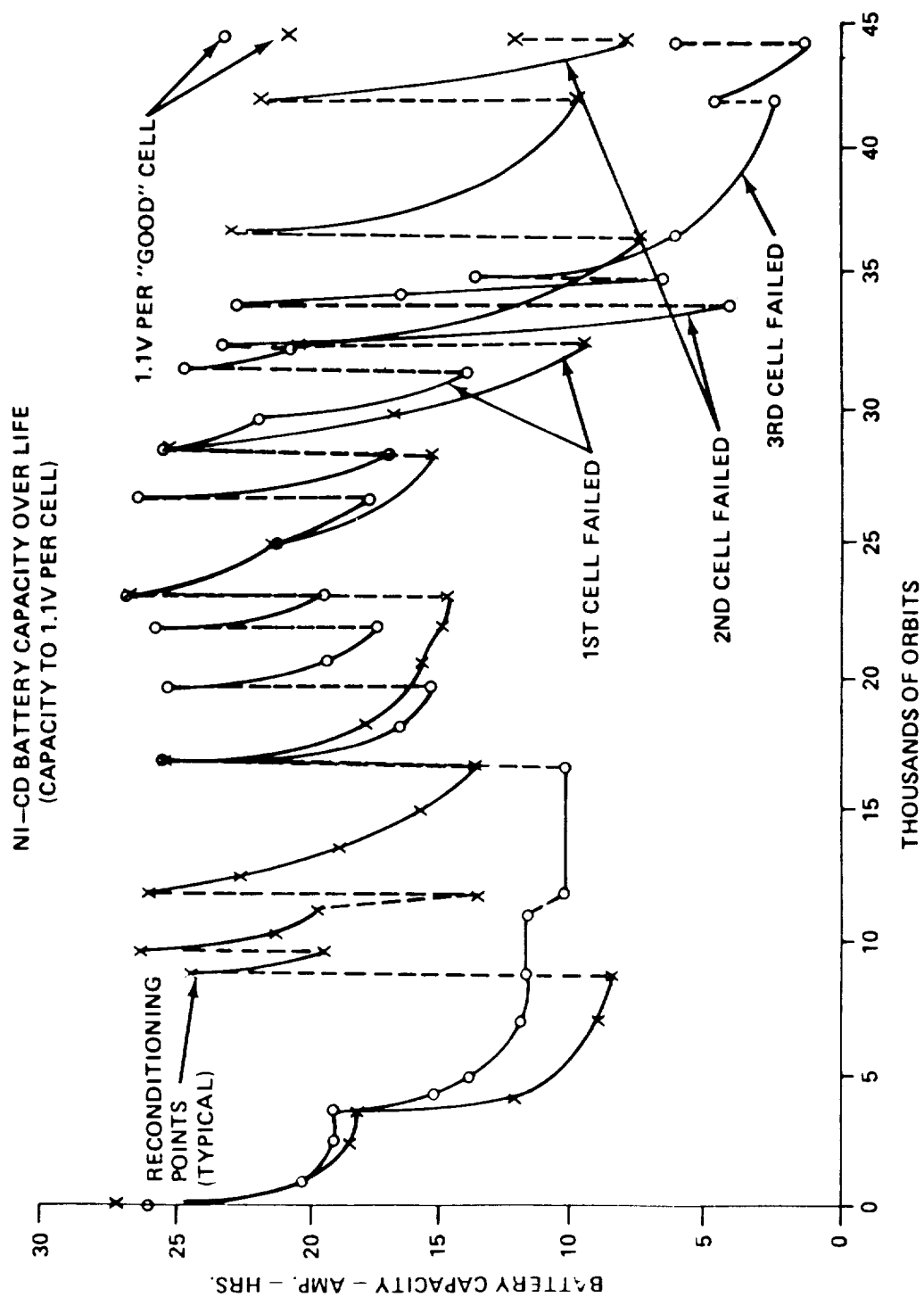
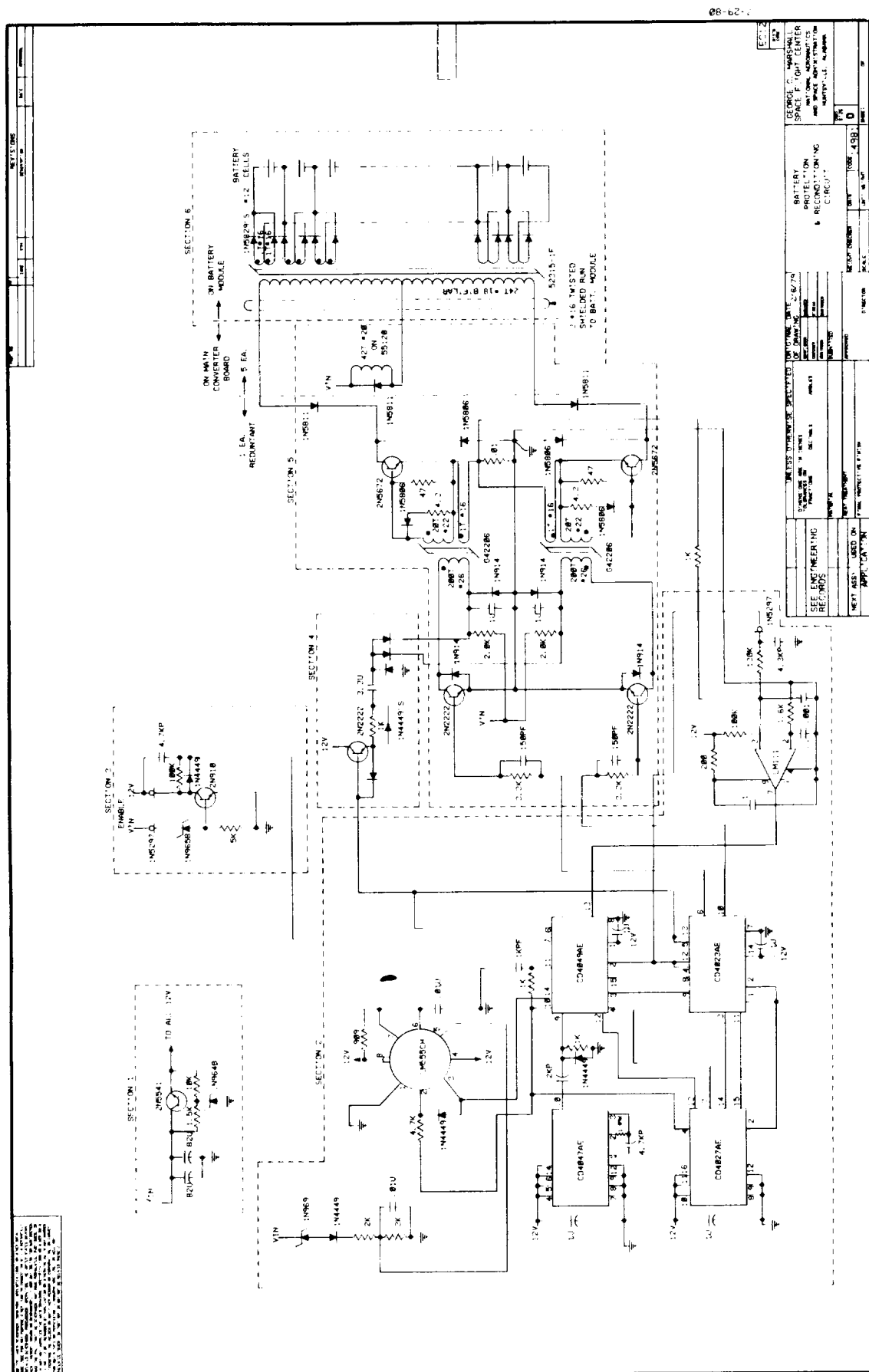


Figure 1. Batteries capacity/life history.





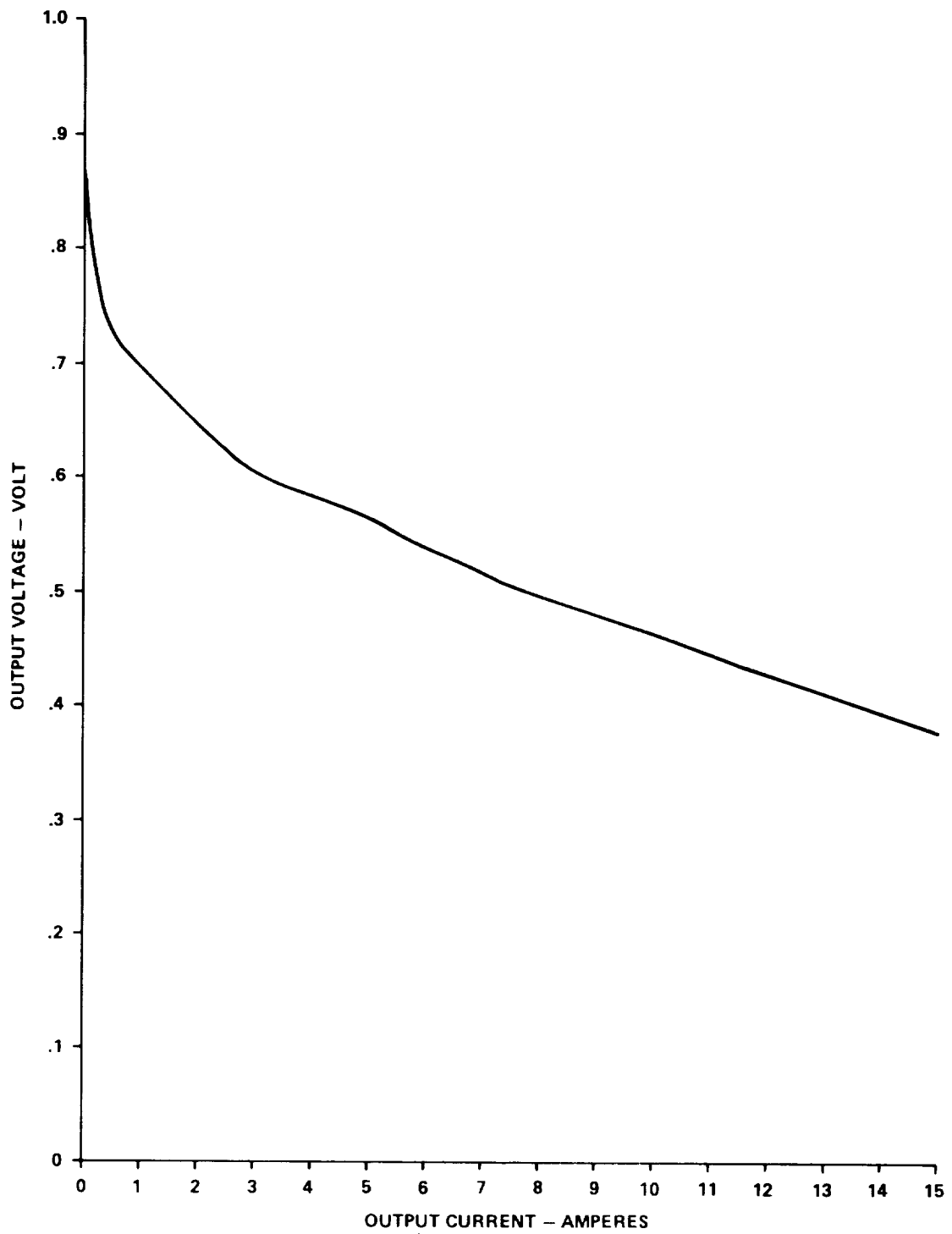


Figure 3. Typical BPRC output characteristic.



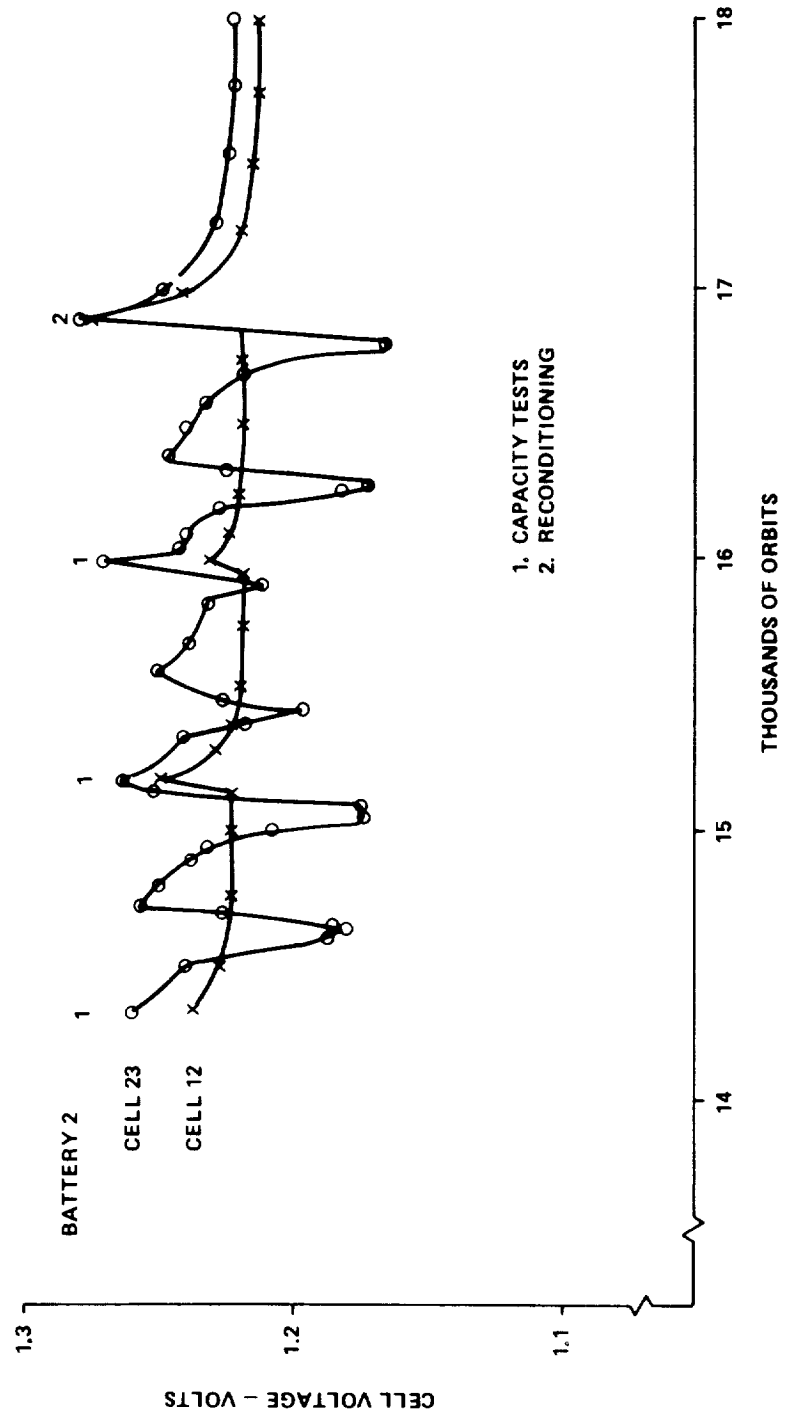


Figure 5. Cell end of discharge anomaly.

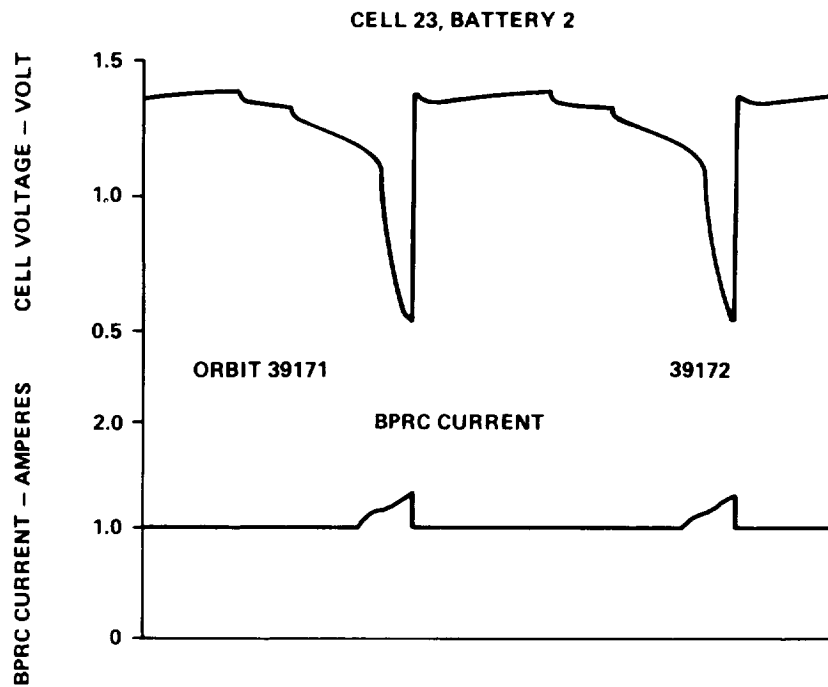
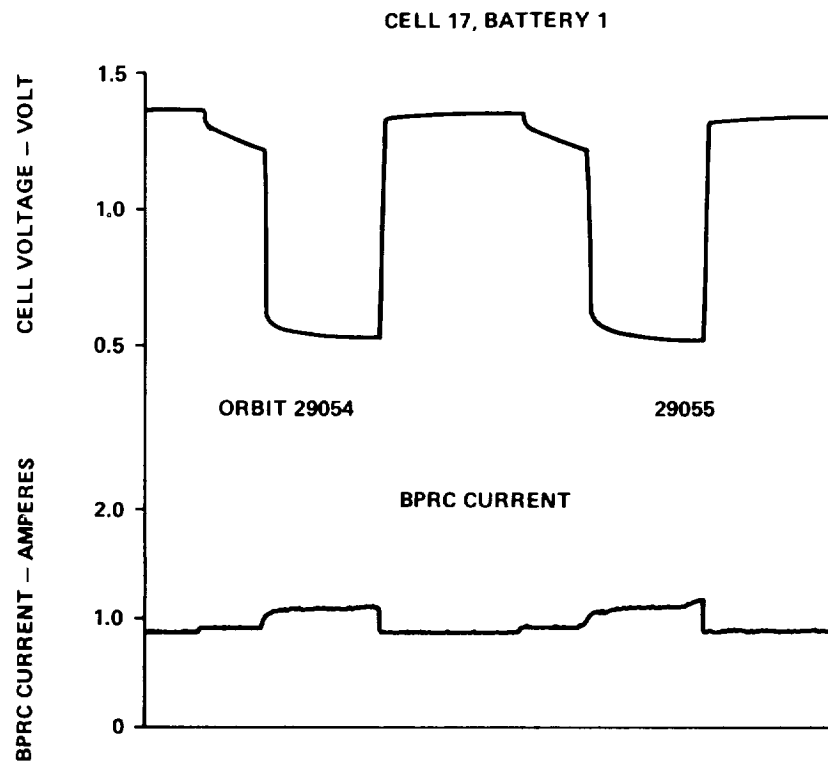


Figure 6. Cell internal leakage anomaly.

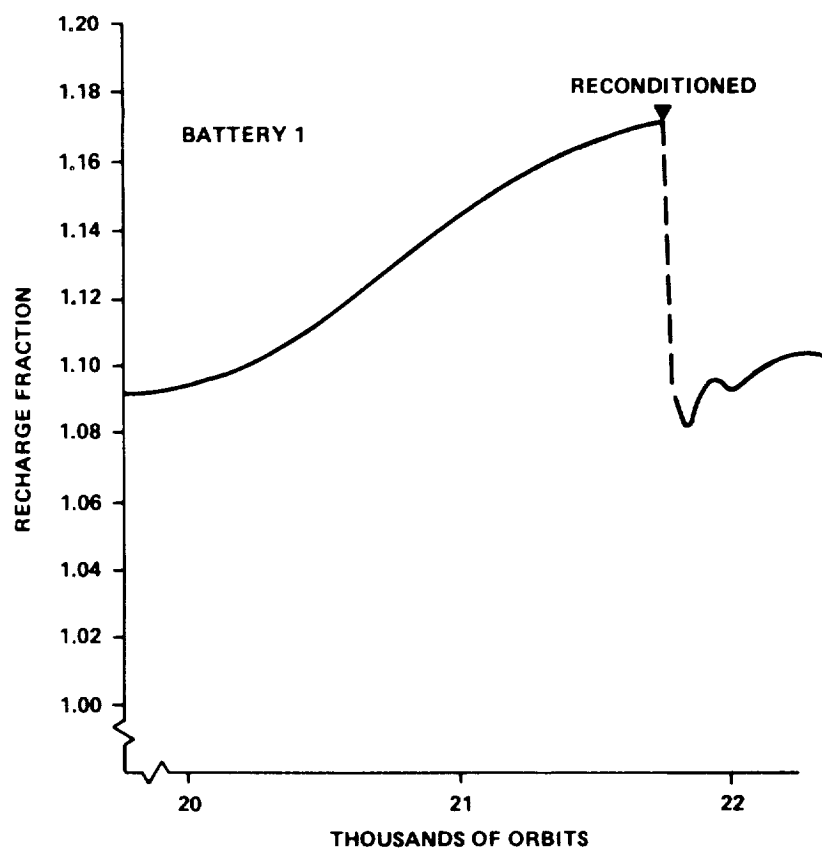


Figure 7. Recharge fraction anomaly.



1. REPORT NO. NASA TP-1873		2. GOVERNMENT ACCESSION NO.		3. RECIPIENT'S CATALOG NO.	
4. TITLE AND SUBTITLE Life Test of a Nickel Cadmium Battery With a Protection/Reconditioning Circuit				5. REPORT DATE May 1981	
				6. PERFORMING ORGANIZATION CODE	
7. AUTHOR(S) John R. Lanier, Jr., and John R. Bush, Jr.				8. PERFORMING ORGANIZATION REPORT #	
9. PERFORMING ORGANIZATION NAME AND ADDRESS George C. Marshall Space Flight Center Marshall Space Flight Center, Alabama 35812				10. WORK UNIT NO. M-350	
				11. CONTRACT OR GRANT NO.	
12. SPONSORING AGENCY NAME AND ADDRESS National Aeronautics and Space Administration Washington, D. C. 20546				13. TYPE OF REPORT & PERIOD COVERED  Technical Paper	
				14. SPONSORING AGENCY CODE	
15. SUPPLEMENTARY NOTES Prepared by Electronics and Control Laboratory, Science and Engineering					
16. ABSTRACT  <p>This report discusses the results of a Ni-Cd battery test over a period of 8 years, 2 months and 44,213 simulated low earth orbits. The battery cells were protected against overdischarge and reversal at discharge rates up to 25 amperes (1.25C) by a battery protection and reconditioning circuit (BPRC). The circuit performed flawlessly during the test, and proved its value, both as a battery reconditioner and a cell protection device. Battery cell failures are also discussed. The test demonstrated the viability of using Ni-Cd batteries at depths-of-discharge up to 25 percent for over 5 years in a low Earth orbit.</p>					
17. KEY WORDS  Ni-Cd battery, Electrical Power System (EPS), battery reconditioning, cell protection, low Earth orbit			18. DISTRIBUTION STATEMENT  Unclassified - Unlimited   Subject Category 20		
19. SECURITY CLASSIF. (of this report) Unclassified	20. SECURITY CLASSIF. (of this page) Unclassified	21. NO. OF PAGES 18	22. PRICE A02		

For sale by National Technical Information Service, Springfield, Virginia 22161

NASA-Langley, 1981